AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph [0018] of the application as indicated below:

[0018] The cache 21 is accessed from ~~a~~ an effective address register 19 containing an effective address ~~19~~. The effective address register 19 contains data representing a tag associated with each line of memory in way 0 and way 1, a line index and a byte number. The Line Index portion of the effective address register 19 identifies which line of the ways is to be accessed, and the byte identification data permits selection of a particular byte contained in a line of data.

Please amend the paragraph [0019] of the application as indicated below:

[0019] For each line or row of data contained in way 0 and way 1, a tag in a corresponding row of tag memories 22 is provided. The Line Index addresses both tag memories and both ways 0, 1. The tag data stored in tag memories 22 identified by the Line Index is compared with the effective address register 19 tag data to determine which way contains data defined by effective address register 19. The tag memory producing a tag which corresponds to the tag in effective address register 19 corresponds to the way containing the desired data. In the event that neither tag memory 22 produces a corresponding tag, a cache miss occurs and the data must be recovered from the system main memory.

Please amend the paragraph [0020] of the application as indicated below:

[0020] Using a conventional translational look aside buffer 23, the tag information from effective address register 19 can be reduced to an effective page number and a real page number corresponding to the tag associated with a row of memory in way 0, and way 1. Comparators ~~24~~ 24A and ~~25~~ 24B identify one of the ways of the cache memory array 21 when one of the tag memories 22 produces a tag corresponding to the tag obtained from the effective address register 19. Decoder 17 and decoder 18 are connected to tag memories 22 and the effective address register 19, respectively.

Please amend the paragraph [0021] of the application as indicated below:

[0021] The cache memory array may be operated in either a power efficiency access mode, or in a high speed access mode. The power efficiency access mode is illustrated in FIG. 2. Clock pulses CLK0 or CLK1 are applied to only one of the ways. The selection of which way is to be clocked to produce data is made based on the determination of which way includes the data defined by the effective address register 19. When the access cycle is slow enough to permit a single way to be clocked, and data is produced prior to the end of the access cycle, only one of the ways (shown as way 0 in FIG. 2) is clocked if a hit is determined. A further selection of an individual byte in the data selected by multiplexer 25 is possible by the select circuit 30 in accordance with the byte data contained in the effective address register 19.

Please amend the paragraph [0023] of the application as indicated below:

[0023] When the microcomputing system is running an application which permits the power efficiency mode to operate, based on an assessment that sufficient cycle time is available to permit identification of the way containing the data defined by the line index of the effective address register 19, only one of the ways 21 is clocked if a hit is determined.